Proteus WorkBench

Productivity environment for OPC development and optimization

Overview

Proteus WorkBench (PWB) is Synopsys' powerful cockpit tool for development and optimization of Proteus-based mask synthesis solutions. It is based on an effective hierarchical GDSII/OASIS layout visualization and analysis engine, providing a comprehensive environment for lithography simulation, compact model building, full-chip optical proximity correction (OPC) recipe tuning, layout verification, and mask synthesis flow development.

PWB offers an easy to use platform with access to a wide-ranging set of tools, enabling fast calibration of accurate models, supporting the optimization of highly efficient Proteus recipes for deployment in OPC and verification.

As state-of-the-art lithography exposure tools are operated at their physical resolution limit, new mask and process technologies are being deployed to further shrink features relevant for pattering at advanced technology nodes. Consequently, the requirements for optical proximity correction (OPC) and verification become increasingly challenging. Compact models calibrated against large experimental datasets need to accurately reflect the lithographic performance for a wide range of designs, and correction recipes need to be optimized with respect to a growing number of parameters.

With Proteus WorkBench (PWB), Synopsys provides a single environment that facilitates model building, Proteus OPC recipe generation and optimization, layout visualization and editing, verification, and supports the development and assessment of resolution enhancement techniques (RETs). PWB combines ease-of-use with high efficiency, resulting in a fast turnaround time for setting up production-ready mask synthesis flows.

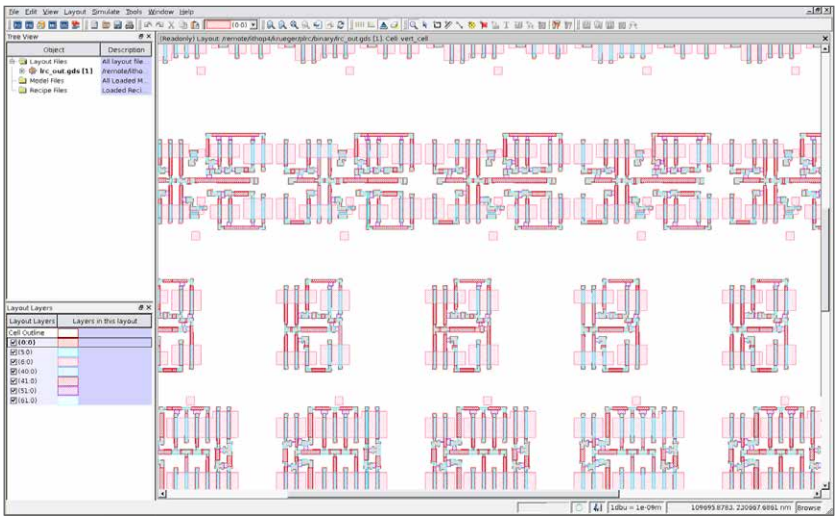

Figure 1: Proteus WorkBench—main user interface

Benefits

- Enable high-speed layout visualization and lithographic performance analysis
- Save engineering time through automation
- Optimize parameters for unmatched full chip OPC and RET performance
- Interface with Synopsys' rigorous lithography process simulation suite, Sentaurus Lithography (S-Litho)

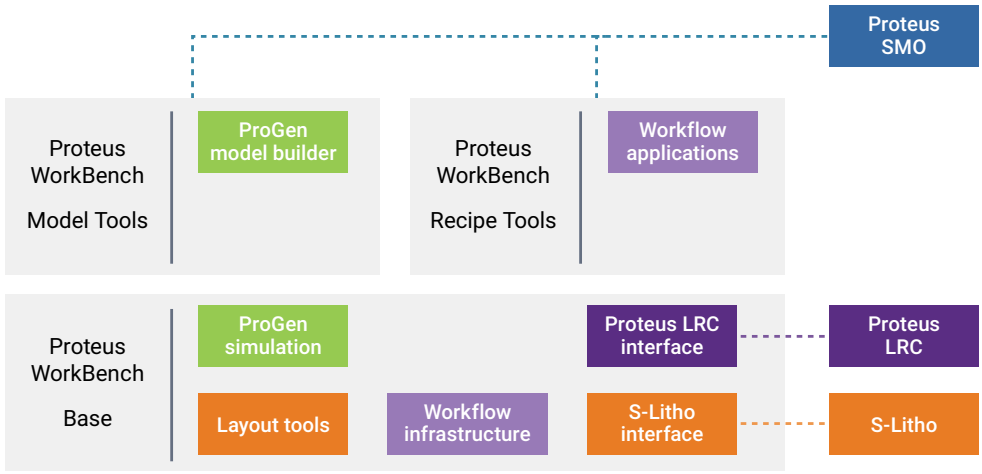

Figure 2: Proteus WorkBench module structure

Layout Tools

Layout Editing, Viewing, and Analysis

PWB is a powerful, hierarchical layout visualization and analysis tool, able to load gigabytes of data in GDSII or OASIS format within minutes. It offers easy exploration by fast zooming and panning capabilities, and allows users to interactively create and manipulate layout patterns to explore advanced OPC solutions.

PWB implements the latest in user interface technology and is architecture to make powerful capabilities easy and intuitive to use. It supports a hierarchical folder representation of all objects including layout, rulers, and other markups such as SEM images. Those can also be overlaid and aligned with layout to enable a comparison with silicon data.

Hierarchy Selection, Editing and Debug

Hierarchical selection and editing allow users to select and edit shapes deep in the hierarchy without requiring the sub-cell to be opened. Edit operations have undo and redo support. In addition, users can overlay two or more layouts in a single view without merging the underlying layout files.

Debugging layouts and their hierarchy is critical for the final design of large chips, and PWB provides a number of tools to do this.

ProGen Simulation

Efficient Litho Contour Generation

Highly accurate ProGen models—the same models used by all Synopsys mask synthesis tools—can be applied within PWB to quickly determine contours or aerial images for a selected layout clip. This lithographic response allows a user to explore advanced OPC techniques or compare OPC performance under different model conditions, helping to evaluate the effectiveness of different RET strategies.

S-Litho Interface

Predictive, Layout Centric Lithography Process Simulation

With shrinking process windows, rigorous lithography process simulation plays an increasingly important role in manufacturing applications. PWB offers a seamless integration of Sentaurus Lithography (S-Litho) into its layout-centric environment. Rigorous simulation enables precise and reliable prediction of the lithographic outcome of both, process and layout variations.

Results such as resist contours or 3D resist profile information can be directly visualized together with the layout information. Process window characteristics are determined, and contour bands can be used to display the corresponding results in PWB.

S-Litho serves as an ideal hotspot validation tool for most critical areas or process conditions, and can be fully integrated into the Proteus LRC verification flow, where results can be easily reviewed using the Proteus Error Analysis Module (PEAM), as shown in Figure 3.

Moreover, PWB provides a comprehensive user interface to the S-Litho Resist Calibrator (SRC), an easy to use environment to determine rigorous resist model parameters. These “resist models” are found by matching simulation results such as critical dimensions (CDs) and profile cross sections to experimental data. For advanced processes, a calibration is mandatory as it is influenced by fab-specific exposure, resist process, and metrology characteristics.

Proteus LRC Interface

Layout Verification—Environment for Setup and Error Analysis

PWB provides and easy-to-use environment to support verification engineers to setup up recipes and review errors reported during the lithography rule check (LRC).

The Proteus LRC recipe setup GUI incorporates best practices for reduced human errors and fast deployment. It guides the user through the definition of relevant input layers and models, supports an interactive feature classification, and helps with the setup of 2D and 3D checks.

PEAM provides an intuitive and feature-rich GUI environment for driving to error locations, reviewing histograms, statistical summaries and process window analysis of the results. Errors can be sorted and filtered, classified, plot, and lithography modeling performed at those locations, either using a ProGen compact model or rigorous simulation by S Litho (See Figure 3). For more information, please see the Proteus LRC datasheet.

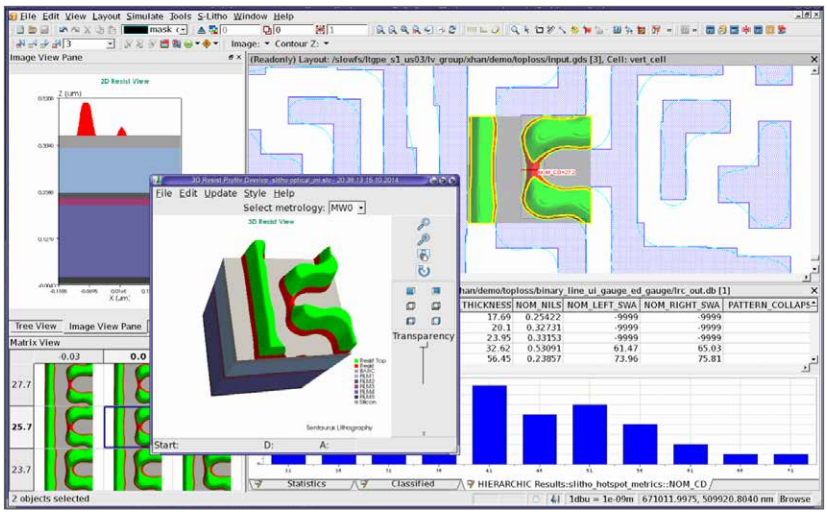

Figure 3: Proteus Error Analysis Module (PEAM) with link to S-Litho results

Workflow Infrastructure

Productivity Platform for Standard or Custom Flows

PWB provides a comprehensive flexible, and easy to use environment to set up and run flows by connecting various Synopsys tools, enabling the conception of custom applications. Users can modify and run pre-defined flows, as well as build new flows based on components available in the library.

Basic infrastructure components for setting up a parameter exploration or optimization are available, including tools for computational resource allocation and flow parallelization. Visualization and analysis of results are supported through flexible plotting and charting capabilities.

For instance, a basic One Pass Correction flow allows users to run OPC or lithography rule checks (LRC) interactively on a selected layout clips, using the Synopsys Proteus toolset. Correction and/or verification recipes are applied to the selected patterns, helping users to explore the impact of recipe parameter variations, to review the an OPC result, or to assess hotspot fixes interactively.

PWB offers a collection of powerful tools that allow engineers to further improve the quality of results of Proteus-based mask synthesis flows. Through the PWB toolbar, users can easily access those applications and load specific GUI elements. The entire working environment can be customized; menus and toolbars can be modified. PWB is fully programmable, allowing users to add own macros and scripts to extend functionality, turning PWB into a unique tool box to address individual engineering tasks.

PWB Model Tools

Progen Model Builder—Shortest Time to Accurate Models

ProGen models are empirical compact models reflecting the performance of a lithography process. Model parameters are determined by fitting experimental data. The ProGen Model Builder (PMB) provides an individual tool set for calibrating those parameters with a high degree of automation, and tuning them for optimum performance. Compared to the stand-alone ProGen application, PMB significantly reduces the time to build models, while maintaining the high accuracy standards of expert-calibrated models.

A newly designed user interface guides the user through the individual model building steps, e.g. defining the lithographic process conditions, test patterns, and locating empirical data. Pre-defined search algorithms and cost functions, as well as best practices, are built into the calibration routines to generate highly accurate models for use in OPC and RET.

Moreover, users have the flexibility to apply weights, modify cost function, or adjust regression types. Input data as well as intermediate calibration and validation results are stored in a database for easy access, and comparisons. Distributed processing schemes can be adjusted to minimize the turnaround time. Figure 4 shows a the PMB user interface including its powerful model analysis and plotting capabilities.

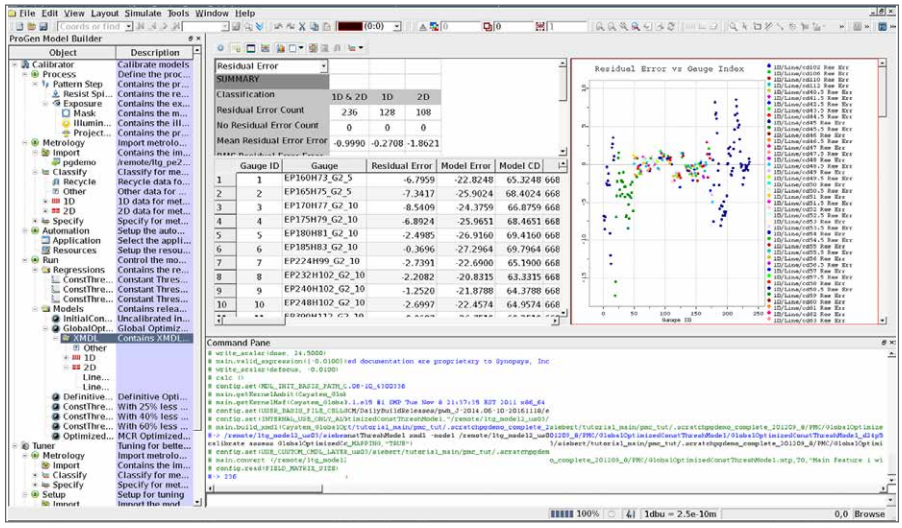

Figure 4: ProGen Model Builder (PMB) user interface

Metrokit—Design-Based Metrology Automation

MetroKit is a toolset designed to facilitate and automate the process of interfacing with metrology tools, thereby minimizing tool downtime and maximizing engineering efficiency. The module provides the ability to generate parameterized test patterns for model building and layout an entire test photomask, as well as to automate the creation of metrology recipes for CD SEM data collection. Moreover, it supports the import and analysis of metrology data, visualization, flyer detection and elimination. Users can create gauge files for model tuning and contour characterization. Reformatted data sets are provided to other Proteus applications to ensure a seamless deployment of metrology information.

PWB Recipe Tools

Efficient Access to Workflow Applications

PWB Recipe Tools enables a cost-efficient access to a wide range of Proteus-based application flows. It helps users to allocate computational resources for distributed processing of exploration or optimization tasks across multiple cluster nodes. At the same time, PWB Recipe Tools enables a flow specific licensing mode for Proteus components used in the flows, efficiently controlling the access to Proteus production tools for OPC and RET development.

Recipe Parameter Tuning

The Recipe Parameter Tuning (RPT) flow represents a simple as well as effective application flow, enabled through the Workflow infrastructure. For a given set of test pattern or critical layout clips, users can vary multiple recipe parameters over a wide range, apply OPC, and assess the corresponding result through a manufacturing-proven lithography rule check. The basic flow is outlined in Figure 5, showing the setup within the Workflow environment, with the components used to realize this application.

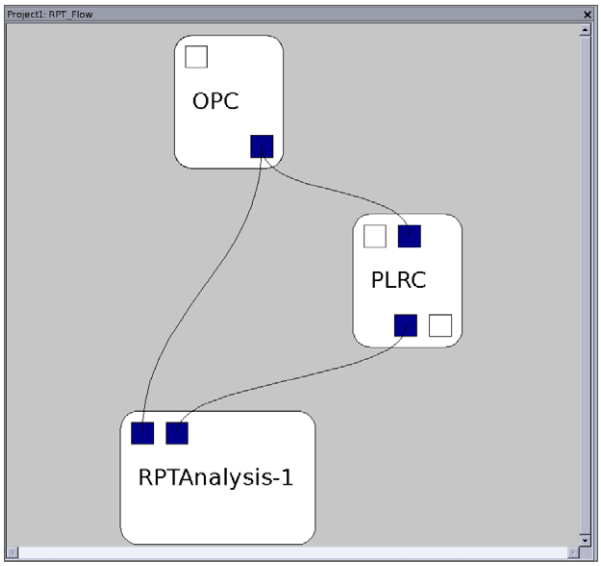

Figure 5: Recipe Parameter Tuner (RPT) application flow

Extensive charting and plotting tools, embedded within the Workflow environment, support the analysis. Distributed processing can be easily utilized to minimize run time, enabling users to explore a large parameter space in order to optimize recipes for deployment in conventional OPC as well as ILT (invers lithography technology).

Proteus SMO

Proteus Mask Treatment Enables Full Chip Optimization

The Workflow infrastructure of PWB is also used to set up more complex flows such as a Proteus tool based flow for source mask optimization (SMO). For a set of critical patterns or cells, the optimum illumination source shape is determined, while simultaneously the mask is optimized for printability. The cost function can be flexibly defined by the user and incorporates result parameters such as edge placement error, exposure latitude, mask error enhancement factor (MEEF) or process variability parameters such as PV-bands. Parameterized as well as free-form, pixelated source types are supported. For the mask treatment, production proven OPC or ILT recipes are deployed, which ensures a smooth transfer of the SMO specific mask solution to full chip mask synthesis applications.

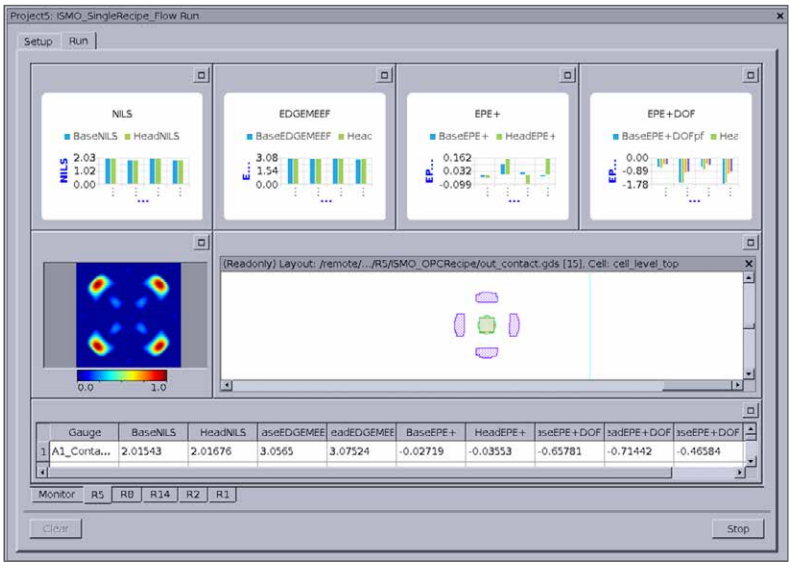

Figure 6: Source mask optimization—Workflow application

The Workflow infrastructure (Figure 6) does not only provide the environment for setting up and running the SMO flow, but also provides powerful visualization and analysis capabilities, guiding the engineer through the optimization process. Moreover, the flow and be easily customized to meet the many individual requirements of SMO applications.

For more information about Synopsys products, support services or training, visit us on the web at: synopsys.com, contact your local sales representative or call 650.584.5000.