SYNOPSYS®

DATASHEET

PrimeTime

Golden Timing Signoff Solution and Environment

Overview

Signoff users have a few key requirements for their signoff tool of choice: runtime and capacity to handle their largest chip size requirements, efficient multi-scenario analysis to verify timing across all corners and modes, margin control to reduce over-design and maximize chip performance, and accuracy to ensure correlation to silicon.

The Synopsys PrimeTime® Suite addresses these requirements by delivering fast, memory-efficient scalar and multicore computing, and distributed multi-scenario analysis and ECO fixing, while using variation-aware Composite Current Source (CCS) modeling that extends static timing analysis (STA) to include crosstalk timing, noise, power and constraint analysis.

PrimeTime Suite

The Synopsys PrimeTime suite, including PrimeTime, PrimeTime SI, PrimeTime ADV, and PrimeTime PX, provides a single, golden, trusted signoff solution with smarter approaches to timing, signal integrity, power, timing constraint and variation-aware analysis. It delivers HSPICE® accurate signoff analysis which helps pinpoint problems prior to tapeout, thereby reducing schedule risk, ensuring design integrity, and lowering the cost of design. This industry gold-standard solution improves your team's productivity by delivering fast turnaround on development schedules for large and small designs while ensuring first-pass silicon success through greater predictability and the highest accuracy.

Benefits

HSPICE-Accurate Results Minimize Over-Design

HSPICE-accurate analysis pinpoints timing problems quickly and reduces ECO fixing time. Use of CCS models provides consistent results for static timing, signal integrity, power, and variation-aware analysis. Path-based analysis is available to zero-in on your most challenging timing paths. On-chip variation modeling and variation-aware analysis deliver additional margin control. This helps designers avoid the over- and under-design of chips, reducing costs and saving time from design schedules.

Integrated Design Environment Improves Productivity

The unified analysis environment in the PrimeTime Suite enables designers to perform complete timing, signal integrity, timing constraint, power and variation-aware analysis in a single environment. This improves designer productivity, reduces set-up steps, and minimizes the number of interface files created and used. It also leads to faster time-to-results because identical operations, such as timing and slew calculations, are not repeated. Costs are minimized by eliminating the need for multiple point tools with associated support costs.

Fast Turn-Around Time

PrimeTime offers a range of solutions to reduce the time required for analysis and signoff. Highly scalable multicore support reduces the time required for static timing and signal integrity analysis by taking advantage of the runtime benefits of threaded parallel processing. Distributed Multi-Scenario Analysis (DMSA) allows multiple scenarios to be run concurrently, which reduces wall clock time and produces a single comprehensive timing report.

High Capacity

PrimeTime performance and capacity improve release over release to take full advantage of the latest multicore compute hardware available in server farms. PrimeTime uses disk-caching for scalable multi-threading delivering fast performance in a low memory footprint.

Comprehensive Signoff

Comprehensive timing and design rule checking, extensive design constraint annotation and delay reporting allow ASIC and COT designers to signoff with confidence knowing that all aspects of their designs have been analyzed.

Advanced Node Support

PrimeTime supports the latest process node requirements at 7-nm and below, including advanced waveform propagation technology that accurately models waveform distortion at advanced nodes, especially in ultra-low voltage FinFET technology.

PrimeTime SI

The Synopsys PrimeTime SI static timing analysis solution is the most trusted and advanced timing signoff solution for gate-level designs. It is the standard for gate-level static timing analysis with the capacity and performance for 750+ million instance chips being designed at 10-nm and below. With shrinking process geometries and rising clock frequencies for nanometer designs, signal integrity (SI) effects such as crosstalk delay and noise (or glitch) propagation can cause functional failures or failed timing. The PrimeTime SI solution provides accurate crosstalk delay, noise (glitch), and voltage (IR) drop delay analysis to address signal integrity effects at 90-nm and below.

The PrimeTime SI STA solution provides designers with extensive timing analysis checks, on-chip variation analysis techniques, golden delay calculation, advanced modeling, unmatched productivity and ease-of-use, a graphical user interface and industry-wide ASIC vendor signoff and foundry support.

The PrimeTime SI static timing analysis solution provides the foundation and environment for a suite of extensions in signoff analysis. In addition to timing analysis, PrimeTime ADV and PrimeTime ADVP deliver extensions for multi-voltage analysis, enhanced hierarchical support, distributed analysis, advanced ECO guidance and variation-aware analysis, and leakage and dynamic power analysis.

Golden Delay Calculator

PrimeTime's built-in RC delay calculator uses parasitic information and CCS libraries to calculate cell and interconnect delays with SPICE-like accuracy. The delay calculation and parasitic annotation reporting capabilities enable designers to debug and pinpoint timing problems. The PrimeTime delay calculator supports voltage and temperature scaling between libraries. This enables multi-voltage analysis without the need to maintain a large collection of libraries for each unique Process Voltage Temperature (PVT) point.

Advanced On-Chip Variation (AOCV) Analysis

At 65-nm and above, the traditional approach of using a global derate margin to account for on-chip variations (OCV) can provide margin control to account for process variation. At process nodes below 65-nm, PrimeTime's AOCV modeling capability extends OCV analysis to deliver an improved method of adding margin in a design. AOCV uses context-specific derate factors that consider location and logic depth of each path being analyzed, providing a more accurate method of assigning on-chip variation margins.

Advanced Latch Analysis

PrimeTime provides analysis of the latch-based designs used in power-sensitive applications. Both PrimeTime timing analysis and ECO guidance take the timing characteristics of latches into account. Support for advanced latch analysis allows ECO fixes to be appropriately distributed up- and downstream from latches.

Distributed Multi-Scenario Analysis (DMSA)

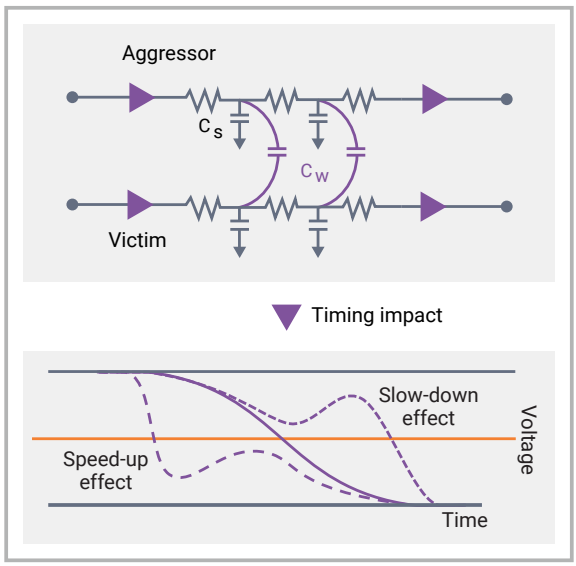
Signoff verification requires analysis of many individual scenarios that represent different operational modes and PVT corners. Analyzing and managing the analysis of these scenarios is simplified with PrimeTime's Distributed Multi-Scenario Analysis (DMSA) capability. DMSA allows designers to run distributed timing analysis simultaneously across multiple scenarios, thereby reducing overall turnaround time. Accompanying visualization capabilities accelerate the debug of multi-scenario analysis results.

Comprehensive SI Analysis

The unified approach of signal integrity and timing analysis delivers a comprehensive and efficient method to analyze noise and crosstalk delay effects on timing. Analysis in a single tool enables faster results while improving designer productivity.

Accurate Crosstalk Delay, Noise (Glitch) and IR Drop Analysis

Signal integrity effects are interdependent and need to be analyzed in the context of timing. PrimeTime SI uses an integrated delay calculation engine with the PrimeTime STA engine to accurately model and compute timing deviations due to crosstalk and IR drop (See figure 2). PrimeTime SI has the capacity and performance to perform accurate noise calculation, detection, and propagation on the largest designs today.



Simultaneous Multi-Voltage Aware Analysis

Multi-voltage designs require exhaustive analysis of cross voltage domain paths to ensure all worst-case paths are identified under all voltage combinations. Simultaneous multi-voltage aware analysis (SMVA) completes analysis of all cross-domain paths under all voltage scenarios in a single run, without the need for margining that can add pessimism.

HyperScale

With HyperScale, PrimeTime allows users to easily migrate from flat design analysis to hierarchical block-level analysis and full-chip distributed timing analysis, using mainstream compute resources available in private computing clouds. The hierarchical methodology supports both top-down and bottom-up flows, with state-of-the-art, timing-accurate context generation. This enables HyperScale block-level model analysis to be re-used throughout the flow, instead of re-analyzing the same blocks over and over at each level. The 5X – 10X performance and memory improvements reduce both compute resource cost and schedule risk, for current and future designs.

Constraint Analysis

PrimeTime improves designer productivity through look-ahead timing constraint analysis and debug technology tuned for the Synopsys Galaxy Design Platform. Early feedback on constraint quality leads to more efficient runtimes and better quality of results in synthesis, physical implementation and static timing analysis tools.

PrimeTime SI provides an intuitive interactive environment for designers to assess the correctness and consistency of timing constraints. This helps to eliminate trial-and-error iterations during implementation and results in more predictable schedules.

Mode Merging

With increased design complexity available at smaller process nodes, comes the need for additional operating and test modes. This can increase the number of scenarios required for timing closure and signoff. PrimeTime SI mode merging technology identifies superset modes that together replicate how a given design is constrained by the original individual mode constraints.

Mode merging uses the PrimeTime distributed multi-scenario analysis (DMSA) infrastructure, and can be added to an existing PrimeTime setup for a multi-scenario design.

Additional Features in PrimeTime SI

- Extracted Timing Models (ETM)
- UPF (Unified Power Format) support
- Graphical User Interface (GUI) enabling timing analysis and visualization using schematics, histograms, tables, and tree graphs
- Session save and restore
- ASIC vendor signoff and foundry support
- Extensive support for industry-standard input and output file formats
- Reduces false violations by considering slew propagation, timing windows, and logical correlation of signals
- Advanced waveform propagation accounts for waveform distortions at 20-nm and below that can impact timing
- SPICE deck output

PrimeTime ADV

PrimeTime ADV offers advanced technology to extend the scope of signoff-driven ECO closure, and provide a next-generation on-chip variation solution.

Physically-Aware Multi-Scenario ECO Guidance

PrimeTime's signoff-accurate ECO guidance enables a fast ECO closure flow. Optimal fixes for both timing and DRC violations are identified using the composite view available in the PrimeTime multi-scenario timing environment, avoiding iterative bottleneck analysis associated with multi-scenario ECOs. PrimeTime's integrated ECO solution offers timing-aware DRC fixing for maximum capacitance, transition and fanout, and timing fixes that honor DRC.

ECO guidance is resource efficient, working either on a single box or a distributed compute farm. In the event that limited hardware resources are available, ECO can be completed where the number of scenarios is less than the number of available hosts.

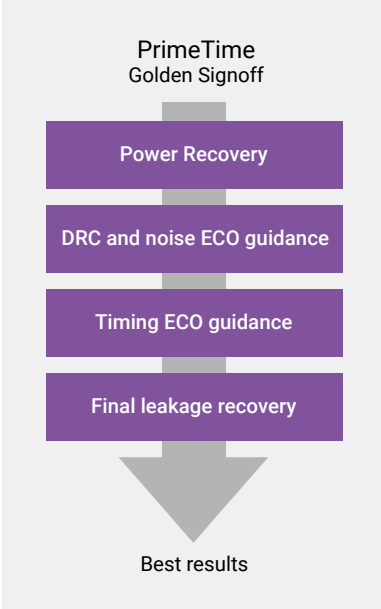
Physically-aware ECO Guidance works closely with IC Compiler's Minimum Physical Impact (MPI) technology, allowing routing and placement-aware timing, noise and DRC violation fixes that accelerate timing convergence by minimizing disruption to an existing layout—something that's especially important for congested designs.

In a hierarchical implementation and signoff flow, PrimeTime provides ECO guidance that complies with physical hierarchy specifications, including multiply-instantiated modules (MIMs) and multi-voltage configurations.

ECO Power Recovery

PrimeTime ECO Guidance can take advantage of positive timing slack to identify power reduction changes to the netlist without creating new timing violations.

PrimeTime ECO power recovery reduces total power and frees up available space for later ECO opportunities. After timing is closed, a final leakage recovery step gains additional power reduction with zero impact to physical design.



Parametric On-Chip Variation (POCV) Analysis

POCV is the next generation of variation analysis targeted at 14/16nm processes and below. It provides a lightweight statistical margining approach to variation margining. It offers Graph and Path-Based Analysis pessimism reduction, along with improved ECO turnaround time. PrimeTime ADV supports early/late LVF input format. In earl/late format, cell arc variation modeling is defined using early sigma and late sigma parameters.

Additional Features in PrimeTime ADV

- Derate-based Multi-input switching support
- Automatically distributed HyperScale STA
- 32-core enabled by single license

PrimeTime ADVP

PrimeTime ADVP offers most advanced technology to extend the scope of timing signoff to 5nm or below, and next-generation on-chip variation solution with moments LVF, multi-voltage and multi-corner optimizations

Enhanced Parametric On-Chip Variation (POCV) Analysis

In POCV is analysis, cell delays and distributions are propagated across the timing graph. Input data required for POCV analysis is provided through Liberty Variation Format (LVF) libraries. Whereas PrimeTime ADV supports early/late LVF input format, ADVP extends the accuracy with moment LVF input formats. In moment format, cells arc variation modeling is defined using mean, mean shift, standard deviation and skewness.

Wire and Via Variation Analysis

PrimeTime ADVP offers complete interconnect variation modeling for metal and via.

For metal variation set_parasitics_derate models global variations by derate factors, such as –resistance_factor, -capacitance_factor and so on. For via variations, modeling includes standard deviations per area for each via layer.

Simultaneous Multi-Voltage Analysis with DVFS

PrimeTime ADVP Simultaneous Multi-Voltage Analysis technology can simultaneously analyze all design paths at all voltage configurations relevant to the path. Reports can be generated for relevant voltage combinations. SMV can also be used along with Dynamic Voltage Frequency Scaling (DVFS) constraints (like clock definitions, exceptions) which can be associated with voltage levels.

HyperTrace PBA

HyperTrace Graph-based refinement technology improves PBA exhaustive runtime significantly. This technology operates on critical region of the timing graph in your design to refine the timing and accelerates PBA exhaustive runtime. The critical region of the design is defined with thresholds for setup and hold slacks.

Machine Leaning (ML based) PBA

PBA with machine learning speeds up PBA exhaustive significantly. This technology automatically trades off runtime vs. accuracy as the design TNS reduces, thereby ensuring it is safe by construction. The machine learning is automatic; No prior training data is required from previous PrimeTime runs or previous PBA commands within the same run.

Cell EM ECO support

PrimeTIme ADVP integrates PrimePower with PrimeTime signoff-driven ECO for the concurrent optimization of power, reliability and timing scenarios. PrimeTime ECO addresses cell EM violations without compromising signoff timing, while providing high fix rate. This is especially critical on the advanced nodes.

Additional Features in PrimeTime ADV

- Physically-Aware ECO Guidance with 7/5nm rules support
- Advanced Multi-input switching support that can model the multi-input switching delays without any pre-characterized MIS data
- Direct database based interface for RedHawk
- Parasitic explorer

Platform Support

OS Platform Support

PrimeTime supports:

- RHEL 6.6+, 7.x, 8+
- CentOS 6.6+, 7.1.1503+, 8+
- SLES 12+, 15+

See the Synopsys Release Specific Support documents for further details.

For more information about Synopsys products, support services or training, visit us on the web at www.synopsys.com, contact your local sales representative or call 650.584.5000