

MVRC

Low Power Static Checker

Overview

Market forces, technology advances and government regulations on green power have made low power design commonplace and necessary for many applications ranging from mobile to plugged-to-the wall devices. Low power design techniques focus on controlling dynamic as well as leakage power and many use voltage control as the guiding principle to achieve power objectives. Low power designs are partitioned into power domains that can have their operating voltage individually controlled. Various modes of design operation translate into one or more power states, where each power state corresponds to a snapshot of the operating voltages for all power domains. Designs employing voltage control techniques pose an ever increasing verification challenge because the design now must be verified in all the specified power states. Further, the low power design needs to be verified throughout the design flow, from RTL to routed netlist.

Low Power Verification Challenge

Architectural design bugs that violate the principles of low power design may exist even at RTL. Such bugs are best detected early on with static checks.

Low power design techniques add new design elements at different stages of the design flow. A Power Gated design includes power switches to turn off power domains and isolation cells to protect unknown values being driven from a powered down domain that communicates with a powered up domain. Isolation cells are typically synthesized automatically. Power switches are added by a place-and-route tool. Insertion and connection of the power switches and isolation cells can be validated by structural static low power rule checks. If a low power design uses Retention to save and quickly restore the contents of a powered down domain, retention register connections need to be validated after synthesis and again after place and route. Multi-voltage designs or designs using Dynamic Voltage Scaling (DVS) have different power domains operating at different voltage values. Level shifters are automatically synthesized to convert voltages of signals traversing such domains, and level shifter insertion and connectivity must be validated throughout the design flow.

For multi-voltage designs, it is important to verify that the appropriate power and ground pins are connected to the specified supply rail. This can also be accomplished by static low power rule checks on a power and ground (PG) connected netlist.

Static check flow

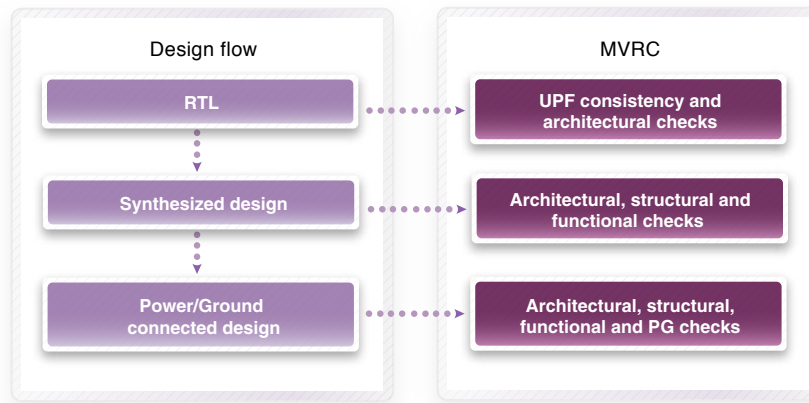


Figure 1: MVRC validates low power implementation throughout the design flow

MVRC

The Synopsys low power solution for static checks includes Formality and MVRC. Formality is a companion product to MVRC that performs equivalence checks between two representations of a low power design. MVRC is a multi-voltage, static low power rule checker that allows engineers to rapidly verify the designs that use voltage control techniques for power management. MVRC also helps to pipe-clean the power intent [IEEE 1801 Unified Power Format (UPF)] before starting implementation of the low power design.

Key features and benefits

- ▶ Power Intent Consistency Checks – Syntax and semantic checks on UPF that help validate the consistency of UPF before beginning implementation
- ▶ Architectural Checks – Global signals violating power architecture can be detected at RTL

- ▶ Structural and Power and Ground (PG) Checks – Validate insertion and connection of isolation cells, power switches, level shifters, retention registers, and always-on cells throughout the implementation flow
- ▶ Functional Checks – Validate the correct functionality of isolation cells and power switches

MVRC Validates Power Intent Throughout the Design Flow

MVRC takes in RTL or gate-level netlist representations of the design in either Verilog or VHDL. It reads the Liberty DB file for definition of special power management cells. It accepts the power intent specified in UPF.

MVRC outputs a log file and an error and warnings report for all violations related to low power static rule checks. The results can also be viewed in a GUI that classifies messages as error, warnings and infos. The GUI facilitates cross-probing of errors which are then highlighted in a schematic view.

Unique value

- ▶ Comprehensive Architectural Checks – MVRC validates the design in its entirety and checks the critical signal networks in the design for the various power modes. These checks help find connectivity related bugs which would cause functional issues.
- ▶ Consistency of power intent – Incorrect power intent will result in incorrect low power design implementation. The UPF consistency checks ensure that the power intent specification driving low power implementation is syntactically and semantically correct.
- ▶ Validation of power up and power down sequences – MVRC validates a specified power up and power down sequence based on an analysis of the UPF. If the sequence is found to be illegal, it predicts a correct one.

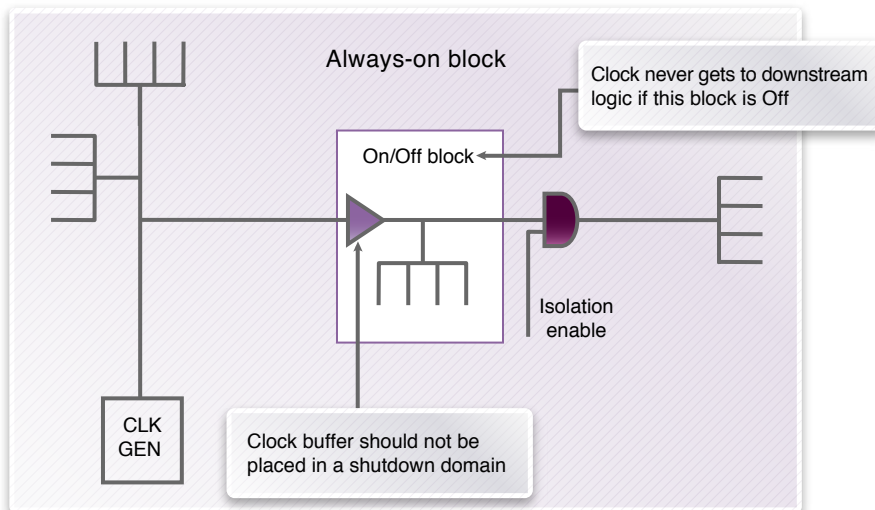


Figure 2: Architectural check example. Clock buffer found in implemented design. Structurally correct, but functionally incorrect.

► Hierarchical power state analysis – Designs with a large number of power domains benefit from the automatic derivation of a hierarchical power-state table. MVRC understands the power intent and is able to prune a large number of power states to a few distinct ones, thus reducing the effort involved to specify and then verify all the power states, transitions and sequences.

An example of a bug that MVRC excels at finding is a clock buffer that has been incorrectly placed in an on/off power domain (see Figure 2). The on/off power domain can be turned off and will be unable to drive the downstream

clock signal in an always-on block. The clock buffer is structurally correctly placed and a verification solution that only checks for correct placement of an isolation cell will fail to detect that this is an error. MVRC is architected for low power and understands the power intent of the chip. It comprehends that this placement is illegal and will likely cause a functional failure. It will report the situation as an error.

Conclusion

Low power design techniques are increasingly used to combat leakage and dynamic power consumption. MVRC's low power static rule checks

understand the power intent and validate implementation throughout the design flow. MVRC is production proven in many customer designs.

For more information about Synopsys products, support services or training, visit us on the web at: www.synopsys.com, contact your local sales representative or call 650.584.5000.