

TetraMAX ATPG

Automatic Test Pattern Generation

Overview

TetraMAX[®] ATPG automatically generates high quality manufacturing test patterns. It's the only ATPG solution optimized for a wide range of test methodologies and integrated with Synopsys' patented DFTMAX[™] compression the leading test synthesis tool. The unparalleled ease-of-use and high performance provided by TetraMAX ATPG allows RTL designers to quickly create efficient, compact tests for even the most complex designs.

Key Benefits

- ▶ Increases product quality with power-aware test patterns for high defect detection
- ▶ Reduces testing costs through the use of advanced pattern compaction techniques
- ▶ Increases designer productivity by leveraging integration with Synopsys DFTMAX compression
- ▶ Creates tests for complex and multi-million gate designs

Features

- ▶ Extremely high capacity and performance
- ▶ Multicore support for accelerated run time
- ▶ Integrated graphical user interface and simulation waveform viewer
- ▶ Comprehensive scan design rule checking
- ▶ Integrated fault simulator for functional vectors
- ▶ Yield diagnostics with automatic defect isolation

Options

- ▶ DSMTTest option enables power-aware patterns and advanced fault models
- ▶ IddQ Test option available for quiescent test validation
- ▶ Integrated with Synopsys Yield Explorer for true, high-bandwidth volume diagnostics

Testing Complex ASICs

With TetraMAX ATPG, designers can generate high-quality manufacturing test patterns without compromising on high performance design techniques (Figure 1). While such techniques may impede other ATPG tools, TetraMAX ATPG is able to obtain coverage on the resulting complex logic.

TetraMAX ATPG supports internal three-state busses including implementations with pull-ups, pull-downs and charge storage. Similar to three-state busses, bidirectional I/O pads are also supported. To ensure ATE (automatic test equipment) requirements are met, TetraMAX ATPG provides a number of options to generate contention-free patterns for three-state logic.

Memory Shadow Testing

Logic with fault effects which pass into a memory element, and logic that requires the outputs of the memory to set up a fault, are said to be “in the shadow” of the memory (Figure 2). Typically, the memory’s shadow affects a significant portion of the chip and causes a reduction in fault coverage. TetraMAX ATPG supports behavioral models of the memories to resolve the shadow effects and increase overall fault coverage for the circuit.

ATPG Design Rule Checking

TetraMAX ATPG’s design rule checker (DRC) identifies chip-level test issues. Violations can be analyzed by viewing them directly on the circuit using TetraMAX ATPG’s integrated graphical schematic viewer (Figure 3). Detailed violation information is available with context-sensitive help. TetraMAX ATPG’s fast DRC checks for the following problems:

- ▶ Flip-flops which violate scan chain design rules
- ▶ Asynchronous logic which may increase TetraMAX ATPG runtime or reduce fault coverage
- ▶ Clock generation logic and three-state busses that may be difficult to control during TetraMAX ATPG
- ▶ Test protocols which may cause incorrect behavior on the tester

TetraMAX ATPG’s DRC supports full-scan and partial-scan test methodologies using mux-scan, clocked-scan, level-sensitive scan design (LSSD) and proprietary schemes. For maximum flexibility, TetraMAX ATPG accepts user-defined constraints and initialization patterns required for proper scan chain shifting. Complete support is provided for designs with IEEE 1149.1/6 internal scan shifting protocols and related techniques that minimize the number of external I/O pins required for ATPG.

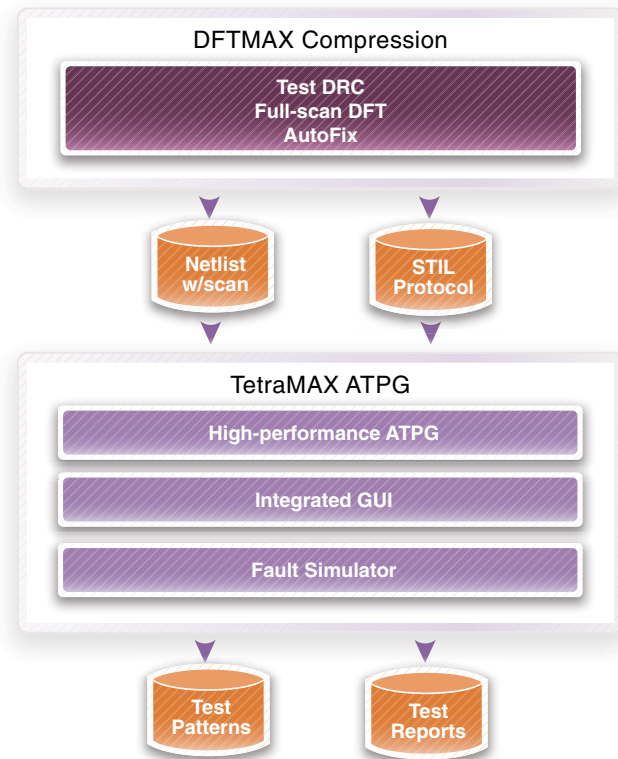


Figure 1: Integrated Test Flow Using TetraMAX ATPG

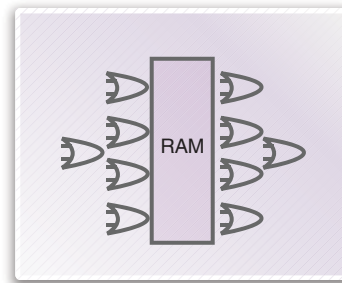


Figure 2: TetraMAX ATPG Delivers High Test Coverage on a wide range of design styles

Pattern Compaction

TetraMAX ATPG uses the most advanced compaction techniques to minimize test pattern count during the ATPG process, even on designs that have many clock domains. With these techniques, TetraMAX ATPG reduces the number of test cycles required to test each device, resulting in lower tester costs.

Deep-Submicron Testing

Many manufacturing defects will not be caught without additional deep-submicron (DSM) testing that specifically targets subtle nanometer defects.

With the TetraMAX DSMTTest option, designers and test engineers can easily generate transition delay, path delay (Figure 4), bridging or dynamic bridging test patterns.

Advanced features unique to the TetraMAX DSMTTest option:

- ▶ PrimeTime® interface selects critical timing paths and timing exceptions
- ▶ Full support for on-chip clocking such as PLLs
- ▶ Easy-to-use flow with graphical support for analysis and debug ATPG algorithms optimized for each specific delay testing mode

- ▶ Pattern merging to maximize delay testing efficiency
- ▶ Tester-ready patterns with complete timing

TetraMAX DSMTest for Small Delay Defect Testing

TetraMAX DSMTest enables ATPG to target subtle small delay defects inside ICs that could lead to failures when devices operate at full speed. Detecting these defects reduces defect levels compared to levels achieved by only using standard transition delay patterns and lowers the cost of production testing.

TetraMAX ATPG accesses precise timing information from Prime-Time, the industry's de facto sign-off static timing analysis engine, to achieve the timing resolution needed to accurately target small delay defects (Figure 5). No unnecessary yield loss occurs because there is no need to test the parts at faster-than-at-speed frequencies. Included with the TetraMAX DSMTest option, small delay defect ATPG provides the following capabilities and benefits:

- ▶ Ultra-high-quality testing
- ▶ Highly-accurate timing information read from PrimeTime
- ▶ One-pass flow:
 - Slack-based ATPG for small delay defects
 - Standard transition delay ATPG for larger delay defects
- ▶ User control of targeted delay defect size
- ▶ Reports and histograms, including:
 - Delay effectiveness metric
 - Statistical delay quality level (SDQL) metric
- ▶ No design or DFT changes needed

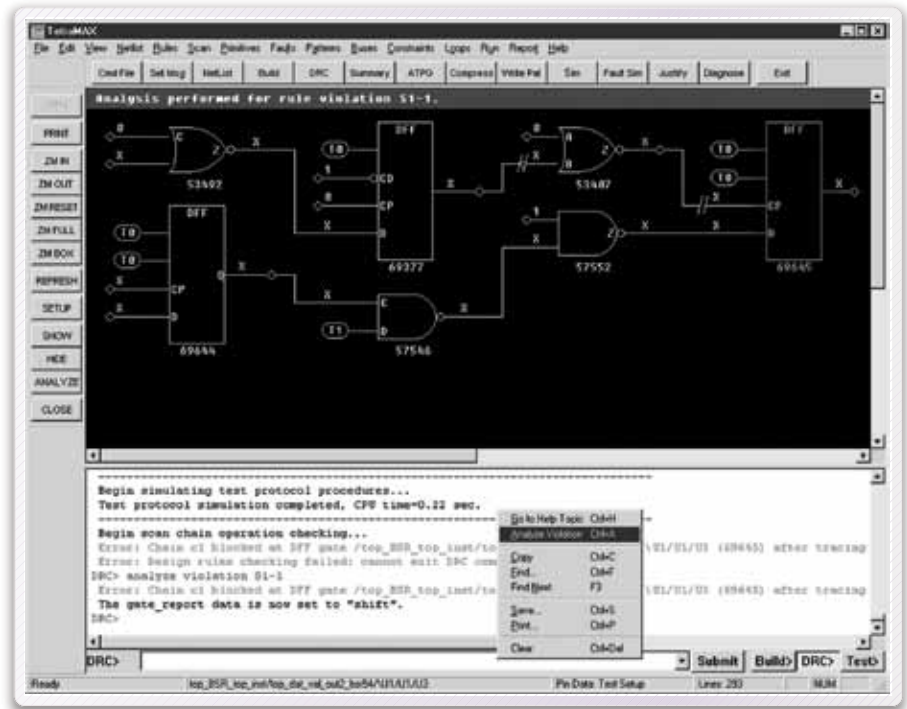


Figure 3: TetraMAX ATPG Provides High-Performance ATPG and advanced debug capabilities through its integrated graphical interface

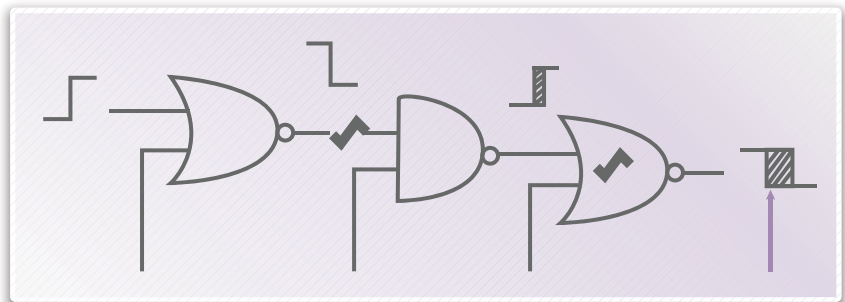


Figure 4: TetraMAX ATPG Delay Test automates testing of critical paths

Power-Aware ATPG

Scan testing typically increases transistor switching activity by many times their peak functional-mode levels, leading to excessive power consumption. Too much power consumption during test can lead to unpredictable test results, including the failure of good devices on the tester, and unnecessary yield loss.

TetraMAX ATPG for power-aware test limits power consumption during test by automatically reducing switching activity to levels consistent with normal operation, based on designer-specified power budgets. This is achieved without compromising test coverage or the cost-savings advantage of DFTMAX compression.

Multicore Processing

For many design teams, turn-around time for pattern generation is critical. TetraMAX ATPG takes advantage of the shared-memory architecture of widely available multicore computing machines to significantly cut the time needed to generate high-quality manufacturing tests. Optimizations in TetraMAX ATPG ensure that runtime performance scales well with the number of processor cores used, reducing runtimes when run on 2 to 32 cores while achieving the same high test coverage and low pattern count from operation on a uniprocessor machine. Multicore processing in TetraMAX ATPG is easily enabled with a single command line switch.

IDDQ Testing

IDDQ testing is a method for enhancing the quality of IC tests by measuring the power supply current of a CMOS circuit. Defect-free CMOS circuits draw very low levels of current during a quiescent state. IDDQ levels are typically an order of magnitude higher in the presence of a silicon defect. IDDQ testing targets physical defects that create a conduction path from the power supply to ground and result in excessive current draw.

TetraMAX ATPG generates a minimal set of high fault coverage patterns for IDDQ testing purposes, and constrains the test patterns to avoid excessive current during the quiescent state. The TetraMAX IddQ Test option then accurately validates these patterns for low quiescence using Synopsys VCS® or other Verilog simulator, thereby ensuring the IDDQ patterns will work on the ATE.

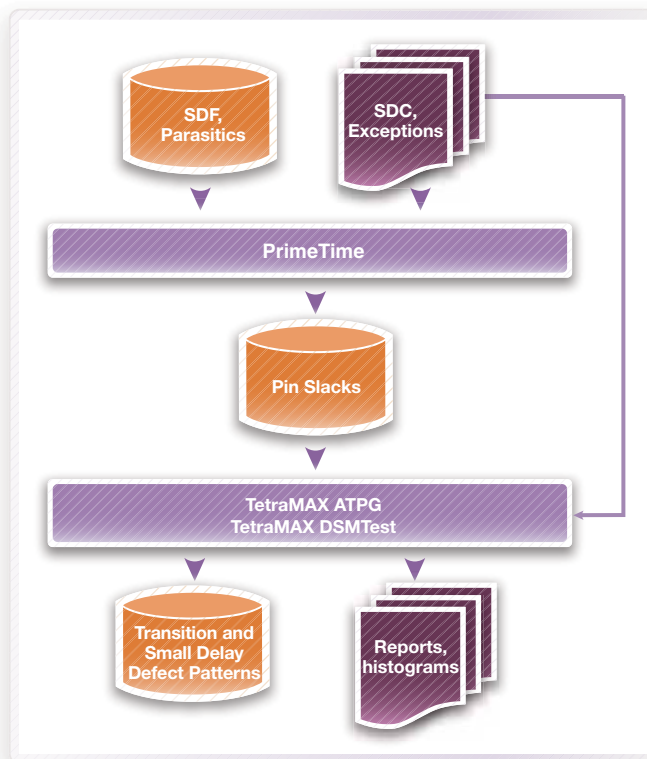


Figure 5: TetraMAX ATPG small delay defect testing flow

Yield Diagnostics

In addition to identifying defective parts from manufacturing, TetraMAX ATPG can also isolate the location of defects on devices that fail TetraMAX ATPG test patterns. Automatic and accurate defect isolation is an important step to diagnose critical yield issues, both during production ramp as well as in volume manufacturing. TetraMAX ATPG diagnostics read the test patterns and tester failure data, which are the differences between measured and expected responses to those test patterns. They also report the fault candidate locations that most likely explain the faulty device behavior observed on the tester. TetraMAX ATPG diagnostics use advanced heuristics and a high-performance fault simulator for rapid and reliable results in a volume manufacturing environment.

Netlist Formats, Testbenches, and Test Patterns Interfaces

TetraMAX ATPG supports popular industry standards for netlist and test pattern formats:

- ▶ Circuit netlist: Verilog, VHDL (87 and 93)
- ▶ Library: Verilog functional (Structural and UDPs)
- ▶ Testbench: Verilog (serial and parallel), VHDL-93 (serial only)
- ▶ Test Patterns: STIL, WGL, Verilog VCDE (input only)

For information related to products, training or support services, please visit the Web at www.synopsys.com. For sales assistance, call 1 650 584 5000.

