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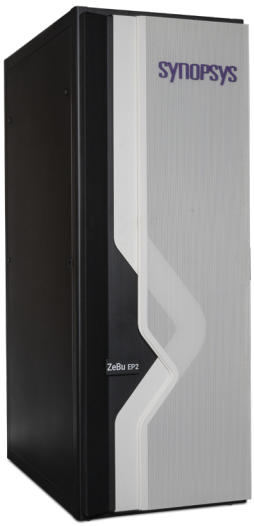
SPEC SHEET

Synopsys ZeBu EP2

Scalable Platform for Emulation and Prototyping



ZeBu EP2 Highlights

- The most scalable, unified platform that supports both emulation and prototyping
- Extends the performance and scalability of Synopsys ZeBu® EP1
- Capacity scaling supports up to 5.8 billion gates
- Highest performance platform supporting petacycle workloads required for complex systems and SoCs
- Support for key hardware-assisted verification use cases including; early RTL verification & regression, SW bring-up, power and performance analysis, and SW/HW validation
- Lowest cost of ownership with single hardware platform

Synopsys ZeBu EP2 is the most scalable unified hardware platform for emulation and prototyping. It leads the industry with the highest performance and capacity scaling to validate long software workloads for billion+ gate designs. ZeBu EP2 builds on the ZeBu EP1 platform while improving the capacity density, and scalability provided by EP1.

Growing software, silicon, and system complexity requires hardware-assisted verification solutions to achieve first pass silicon success. ZeBu EP2's peformance and capacity scaling support the key use cases for verification and validation needed to achieve that success. Along with performance and scalability, Synopsys ZeBu EP2 supports the largest library of transactor models, memory models, and speed adaptors to run demanding workloads such as AI, networking, and evolving architectures.

For more information about Synopsys ZeBu emulation systems contact your Synopsys representative or visit www.synopsys.com/zebu

ZeBu EP2	Specifications
Max Capacity	Up to 1.44 billion gates, single rack Scalable up to 5.76 BG
Max Power	< 10 kW / billion gates
Dimensions	H: 208cm, W: 74cm, D: 129cm
Weight	< 720Kg
ZeBu Software	
Language Support	Verilog, VHDL, SystemVerilog, EDIF gate-level, SystemVerilog assertions, OVL, SystemC
Use Modes	Hybrid with virtual prototypes, simulation acceleration, power analysis, synthesizable test bench, transaction- based emulation, in-circuit emulation, virtual host and devices, virtual tester
Low Power Verification	IEEE 1801 UPF, power domains, power gating, isolation, retention
Power Analysis	RTL average power, gate level average and cycle power
Debug	View all signals anytime with unlimited waveform upload onto host, or limited waveform depth capture by using interactive/batch waveform reconstruction within Verdi
Vertical Solutions	Vertical market solutions spanning transactors, memory models, hybrid solutions, virtual system adaptors and speed adaptors

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